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PAGE 01

#21 / Appeal
Brief
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MSLIN98-002CC

09/251,183

Nov. 20, 2001

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FROM: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

SUBJECT: Serial #: 09/251,183
File Date: 2/17/99
Inventor: Lin, M.S.
Examiner: J. Garcia
Art Unit: 2823
Title: Top Layers of Metal for High Performance IC's

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NOV 23 2001

TECHNOLOGY CENTER 2800

APPEAL BRIEF


Dear Sir:

In response to the rejection of claims 1-3, 11-13, 15-28, 49, 50, 56-80, 62-68, and 70-83 in the above identified application for patent, made in the FINAL REJECTION in the office action, dated May 18, 2001, applicant filed a NOTICE OF APPEAL that was received by the US Patent and Trademark Office on August 23, 2001. Please accept our appeal brief herewith together with the fee of \$320. The commissioner is hereby authorized to charge payment of the above fee associated with this communication to Deposit account No. 19-0033. A duplicate copy of the request is enclosed. No oral hearing is requested.

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.6

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Stephen B. Ackerman, Reg. No. 37,761 Nov. 23, 2001
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Application no. 09/251,183

APPEAL BRIEF**1. Real Party in Interest**

The real party in interest is the Inventor:

Mou-Shiung Lin
28 Ginsan 10 St.
Hsin-Chu, Taiwan, Republic of China

The above address is an updated address (from that filed originally) for the inventor. No assignment has been recorded for this patent application.

2. Related Appeals and Interferences

There are no related Appeals or Interferences.

3. Status of Claims

Claims 1-3, 11-13, 15-28, 49, 50, 56-60, 62-68, and 70-83 are finally rejected. No claims are allowed. Claims 4-10, 14, 29-48, 51-55, 61 and 29 have been previously cancelled.

Claims 49, 50, 56-60, 62-68, and 70-83 have been withdrawn from appeal, and are being re-filed in a Continuation Application.

4. Status of Amendments

The above referenced Final Rejection was mailed from the US Patent and Trademark Office on May 18, 2001. No amendments were subsequently made to the claims, and a Notice of Appeal was mailed on August 20, 2001.

MSLIN98-002CC

Application no. 09/251,183

A concurrent amendment is being filed to cancel Claims 49, 50, 56-60, 62-68, and 70-83, which are being re-filed in a Continuation Application.

5. Summary of the Invention

The invention provides a method of forming a top level of metal interconnections for high performance integrated circuits. An integrated circuit is provided containing a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices, and containing a plurality of first metal lines in one or more layers. A passivation layer is deposited over the interconnecting metallization structure. An insulating, separating layer of polymer is deposited over the passivation layer that is substantially thicker than the passivation layer. Openings are formed through the polymer insulating, separating layer and the passivation layer to expose upper metal portions of the overlaying interconnecting metallization structure. Metal is formed in said openings and to form a top metallization system connected to the overlaying interconnecting metallization structure, wherein the top metallization system contains a plurality of top metal lines, in one or more layers, each of the top metal lines having a width substantially greater than the first metal lines.

MSLIN98-002CC

Application no. 09/251,183

CLAIM 1 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

1. A method for forming a top metallization system for high performance integrated circuits, comprising:

forming an integrated circuit containing a plurality of devices (2) formed in and on a semiconductor substrate (1), with an overlaying interconnecting metallization structure (3) connected to said devices and containing a plurality of first metal lines in one or more layers; (Fig. 1; Page 9, lines 9-15)

depositing a passivation layer (4) over said interconnecting metallization structure; (Fig. 1; Page 9, 20 to Page 10, line 2)

depositing an insulating, separating layer of polymer (5) over said passivation layer (4) that is substantially thicker than said passivation layer; (Fig. 1; Page 10, lines 3-4)

forming openings through said polymer insulating, separating layer (5) and said passivation layer (4) to expose upper metal portions (6) of said overlaying interconnecting metallization structure; (Fig. 1; Page 10, lines 4-8)

depositing metal contacts (7) in said openings; and (Fig. 1; Page 10, lines 9-10)

MSLIN98-002CC

Application no. 09/251,183

forming said top metallization system (10, 11, 12, 13, 14) connected to said overlaying interconnecting metallization structure, wherein said top metallization system contains a plurality of top metal lines (10, 11, 12, 13), in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines. (Fig. 1 and 2; Page 10, lines 13-22, Page 11, lines 1-6, Page 14, last line to Page 15, line 19)

6. Issues

Whether or not claims 1-3, 11-13, and 15-28 are patentable under 35 U.S.C. § 103(a), over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin.

7. Grouping of Claims

The rejected claims stand or fall together.

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8. Argument

Reversal of the rejection of Claims 1-3, 11-13, and 15-28 as being unpatentable under 35 U.S.C. § 103(a), over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin, is respectfully requested, in view of the following arguments.

MSLIN98-002CC

Application no. 09/251,183

One of the great challenges in the semiconductor industry in recent years has been to reduce RC (resistance capacitance) delay in signal lines and IR drop (reduction in voltage due to high resistance) in voltage planes in the complex, multi-level metallization systems now in use. The industry has expended much effort and vast resources and is now beginning to replace the typical metal used, aluminum, with copper, which has a lower resistivity than aluminum. Furthermore, it is exploring the use of and implementing intermetal dielectric materials with a lower K value (dielectric constant) than previous materials. Such low-K dielectrics can reduce capacitance between metal lines. Both of these approaches have typically been implemented in extremely clean (Class 1 or below) and very expensive semiconductor fabrication facilities now being built and used to manufacture integrated circuit wafers - the metal and low-K dielectrics are deposited and patterned prior to a final, passivation layer being formed over the entire semiconductor wafer surface.

As is well known in the art, increasing either the thickness or the width, or both, of conductive lines reduce their resistivity. However, increasing the thickness of metal lines, and the thickness of the dielectric materials formed above and around the metal lines, is limited in the above referenced semiconductor fabrication facilities by the types of equipment and processes used, such as sputtering or chemical vapor deposition. The width of these lines are limited by the current tight packing of lines at any particular metal level, and by the capacitance increase that occurs between metal layers (in the vertical

MSLIN98-002CC

Application no. 09/251,183

direction) if wide lines are used. Thus, metal lines currently used are "fine lines", of narrow width and limited thickness.

The above referenced passivation layer is typically formed of an insulating material, such as an oxide or nitride, that is deposited over the entire top surface of the integrated circuit, after the "fine line" metallization is completed. The passivation layer serves to prevent mechanical and chemical damage during assembly, packaging and use, and is necessary to protect the underlying fine line metal, and semiconductor devices, from moisture, mobile ions and scratching.

Many of the above mentioned problems and disadvantages are resolved by the method of the invention. The invention as claimed provides a method of forming a top level of metal interconnections for high performance integrated circuits, in which the top level metal is formed after passivation of the underlying integrated circuit, and the top level metal lines are formed to a width substantially greater than the first metal lines formed under the passivation. The top layer metal is separated from the underlying integrated circuit and its top passivation by a thick, polymer separating layer. The organic polymer separating layer is inexpensive compared to the inorganic materials used for the fine line metallization dielectrics, and can easily be deposited to thicker dimensions, to reduce capacitance and allow for thicker top level metals. This organic layer of polymer is formed above the passivation layer 4 since the polymer layer 6 could be a source of ion contamination which could affect the underlying devices. The passivation layer 4, as is well known in the art, is a continuous layer overlaying the entire lower fine-line

MSLIN98-002CC

Application no. 09/251,183

metallization system and devices, and protects the lower structures from both ion contaminants and moisture.

The Examiner has cited Bandyopadhyay (US 5,827,776) as the primary reference in the rejection. Bandyopadhyay, either alone or in combination with the other references cited above, however, fails to disclose or render obvious the subject claimed invention. The Examiner has asserted that Bandyopadhyay, et al. "discloses formation of passivation layer 22". However, Bandyopadhyay's layer 22 is not a passivation layer, as a passivation layer is defined (and as is well known) in the semiconductor industry. Please see the attached two references (referred to as Sematech, and Wolf), introduced in the office action response dated April 5, 2001, that give the industry standard definition for a passivation layer. Sematech describes it as "[t]he final deposition layer in processing". See also the Wolf description, which states that "[f]ollowing patterning of the final metal layer, a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging".

In Bandyopadhyay, et al., layer 22 is not a final layer deposited after all metal layers have been formed. It is merely a first (intermetal) dielectric, as defined at col. 5, lines 66-67. Further metal lines, such as metal lines 14 in Fig. 13, are deposited after layer 22. As seen in the Wolf description referred to above, a passivation layer is necessary to protect the underlying fine line metal, and semiconductor devices, from moisture, mobile ions and scratching (such moisture, mobile ions and scratching would

MSLIN98-002CC

Application no. 09/251,183

commonly occur from "above" layer 14, i.e., from layers and/or manufacturing processes formed subsequently, or from external sources. A semiconductor substrate typically performs such a protective role from "below" the layers shown in the drawings). If Bandyopadhyay's layer 22 was a passivation layer, it would not be able to protect layer 14 from moisture and the thin metal lines 14 could, for example, subsequently be consumed by corrosion due to moisture. The actual passivation layer in the Bandyopadhyay structure would have to be deposited above layer 14, perhaps above other additional fine-line metal layers had been formed.

The claimed invention describes the use of a passivation layer (layer 4 in Fig. 1) which is necessary to protect underlying fine-line metallization 3 as well as devices formed on the substrate 1. The method of the invention, as claimed, then continues with deposition of polymer insulating, separating layer 5, and thick, wide line metallization 10/11/12/13 (see Fig. 2), as well as polymer intermetal dielectric 14/16. This top metal system further differentiates the claimed invention from that described in Bandyopadhyay, or the combination of Bandyopadhyay et al. with Yamada '778, Yamada '020, Wolf and Cronin, as the top metal system of the invention does not require further passivation – the thick, wide metal is sufficiently robust that moisture protection is not required.

In the office action dated May 18, 2001, the Examiner cites Yu et al (US Patent 6,130,457) as employing the term "passivation layer" 62 as a layer analogous to layer 22 of Bandyopadhyay. However the use of "passivation layer" in Yu is believed to be an incorrect or, at best, non-standard use of the term. Layer 62 is more properly

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MSLIN98-002CC

Application no. 09/251,183

characterized as an interlevel dielectric. An incorrect use of an industry-standard term in a single patent reference (in which the drafter is permitted to be his own lexicographer) should carry little persuasive weight as compared to the definition found in a technical dictionary created by an industry-wide consortium (see Sematech) or that found in a widely recognized and cited textbook (see Wolf).

Yamada '778 is cited as disclosing top metal lines 89 which are wider than first metal lines 83, and that an oxide insulating, separating layer 15 is formed. However, Yamada '778, either alone or in combination with the other references cited above, fails to disclose or render obvious the subject claimed invention. There is no suggestion or motivation in Yamada '778 of forming two metallization systems, separated by a passivation layer and a polymer insulating, separating layer, as claimed in the instant invention. Yamada '778 merely shows 2 metal layers in which there is a slight difference in thickness and width of the layers. Further, the oxide insulating, separating layer 15 of Yamada '778 is disclosed to be silicon fluoride oxide (at col. 7, line 62), which is an inorganic material, not the polymer separating layer of the invention.

Yamada '020 is cited as teaching an oxide passivation layer over which a nitride is deposited. While it is acknowledged that a passivation layer may be so formed, neither Yamada '020 alone or in combination with the other references cited above, discloses or render obvious the subject claimed invention, for the reasons stated above.

MSLIN98-002CC

Application no. 09/251,183

Wolf is cited as disclosing the use of polyimide as an intermetal dielectric (IMD), and for teaching spin-on glass as an insulating, separating layer. However, Wolf at pages 215-217 teaches some of the disadvantages that have caused the semiconductor industry to not use polyimide as an IMD – two examples are water absorption by the polyimide, and subsequent corrosion of underlying metal lines. Thus Wolf actually teaches away from the use of polyimide as an IMD in a fine-line metallization system. The invention, however, does not teach the use of polyimide as an IMD in the fine-line interconnecting metallization system, but rather as an insulating, separating layer between the fine-line metal (protected by a passivation layer) and the thick, wide line, top metal system above. The use of the passivation layer of the invention prevents moisture and ionic contamination from affecting the fine-line metal and devices, while the thick, wide metal system above the polymer insulating, separating layer is robust enough that moisture does not have a negative effect on reliability. Thus neither Wolf alone or in combination with the other references cited above, discloses or render obvious the subject claimed invention.

Cronin is cited as teaching metal contacts by damascene metal filling. While it is acknowledged that damascene metal filling is well known in the art, neither Cronin alone nor in combination with the other references cited above, discloses or render obvious the subject claimed invention, for the reasons stated above.

MSLIN98-002CC

Application no. 09/251,183

In summary, Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin, fail to disclose or suggest the method of the invention as claimed, and so reversal of the rejection of Claims 1-3, 11-13, and 15-28 is respectfully requested.

CONCLUSION

Applicant requests that the Board of Appeals reverse the holding of the Examiner in finally rejecting the Claims 1-3, 11-13, and 15-28 in the application. Allowance of the claims is requested.

Respectfully submitted,



Stephen B. Ackerman, Reg. No. 37,761

MSLN98-002CC

Application no. 09/251,183

APPENDIX A**COPY OF THE CLAIMS**

1. A method for forming a top metallization system for high performance integrated circuits, comprising:

forming an integrated circuit containing a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and containing a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metallization structure;

depositing an insulating, separating layer of polymer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said polymer insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metallization structure;

depositing metal contacts in said openings; and

MSLIN98-002CC

Application no. 09/251,183

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system contains a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

2. The method of claim 1 wherein said top metallization system connects portions of said interconnecting metallization structure to other portions of said interconnecting metallization structure.

3. The method of claim 1 wherein said top metallization system contains lines that are selected from the group consisting of signal lines, power buses, ground buses or a combination thereof.

Claims 4-10 have been cancelled.

11. The method of claim 1 wherein said passivation layer contains Plasma Enhanced CVD (PECVD) oxide.

12. The method of claim 1 wherein said passivation layer contains Plasma Enhanced CVD (PECVD) nitride.

MSLIN98-002CC

Application no. 09/251,183

13. The method of claim 1 wherein said passivation layer contains a layer with a thickness within a range of approximately 0.15 to 2.0 um of Plasma Enhanced CVD (PECVD) oxide over which a layer with a thickness within a range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

Claim 14 has been cancelled.

15. The method of claim 1 wherein said insulating, separating layer of polymer comprises polyimide.

16. The method of claim 1 wherein said insulating, separating layer of polymer contains polymer benzocyclobutene (BCB).

17. The method of claim 1 wherein said polymer insulating, separating layer is of a thickness after curing within a range of approximately 1.0 to 30 um.

18. The method of claim 1 wherein said polymer insulating, separating layer is spin-on coated and cured.

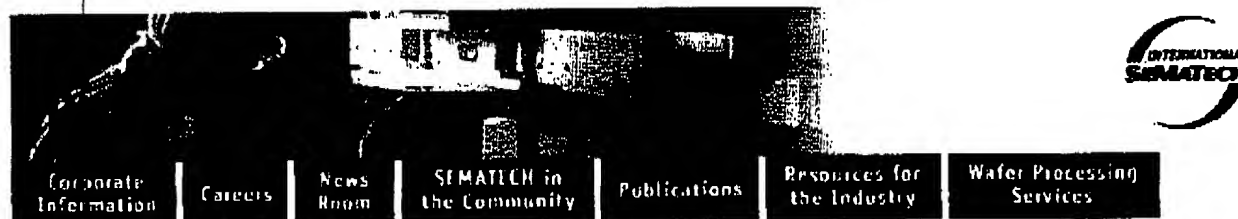
19. The method of claim 1 wherein said insulating, separating layer of polymer is cured at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours, said curing to occur within a vacuum or nitrogen ambient.

MSLIN98-002CC

Application no. 09/251,183

20. The method of claim 16 wherein said polymer insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.
21. The method of claim 20 wherein each of said multiple processing steps of spin on coating and curing is performed at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours, said curing to occur within a vacuum or nitrogen ambient.
22. The method of claim 1 wherein said openings have an aspect ratio within a range of approximately 1 to 10.
23. The method of claim 1 wherein said metal contacts are selected from a group containing sputtered aluminum, CVD tungsten, CVD copper, electroplated copper and electroless nickel.
24. The method of Claim 1 wherein said metal contacts comprise damascene metal filling.
25. The method of claim 1 wherein said top metallization system contains contact pads on a top metal layer whereby said contact pad can contain tungsten, chromium, copper (electroplated or electroless), aluminum or polysilicon.

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SEMATECH DICTIONARY "P - PH"

A-AM | AN-AZ | B | C-CH | CI-COM | CON-CZ | D-DE | DF-DZ | E-EN | EO-EZ
 F-FL | FM-FZ | G | H | I | J-K | L | M-MES | MET-MZ | N | O | P-PH | PI-PQ | PR-PZ | Q
 R | S-SE | SH-SO | SP-STA | STE-SZ | T-TH | TI-TZ | U-V | W-Z

package*n*

a container for a die (often plastic or ceramic) that provides protection and connection to the next higher level of integration. [SEMATECH]

package warpage*n*

the loss of planarity of a plastic molded surface, excluding protrusions and intrusions. In semiconductor packages, warpage is measured by the warp factor. [SEMI G54-93]

packed valve*n*

a shutoff or metering type of valve designed to prevent the gas it controls from escaping to the atmosphere. The escape of gas is prevented by means of a stem that rotates or moves within its seal material during actuation. The dynamic seal interface separates the medium from the atmosphere. [SEMI International Standards 1990, Vol. 1, Glossary]

packet*n*

a physical division of a message used by the message-transfer protocol. NOTE-Each packet contains data and control information. [SEMI E5-92] Also see message protocol.

packless valve*n*

a shutoff or metering valve designed to prevent escape of the gas by a static seal, such as a diaphragm or bellows, that isolates the controlled gas from the atmosphere. [SEMI International Standards 1990, Vol. 1, Glossary]

pad

see bonding pads.

pad-array carrier

see ball grid array.

passivation <i>n</i>	deposition of a scratch-resistant material, such as silicon nitride and/or silicon dioxide, to prevent deterioration of electronic properties caused by water, ions, and other external contaminants. The final deposition layer in processing. [SEMATECH] Also called <i>overcoat</i> and <i>cap deposition</i> .
passive data collection (PDC) <i>n</i>	an activity in which the performance of a process or piece of equipment is sampled while it is running in normal production mode. This activity is used to evaluate normal production mode. This activity is used to emulate normal production without making tweaks or adjustments to the process beyond those normally made during production. [SEMATECH]
passive devices <i>n</i>	semiconductor devices that have passive function, such as capacitors and resistors. [SEMATECH] Contrast active devices.
passive equipment <i>n</i>	equipment that is loaded or unloaded by the active equipment. [SEMI E23-91] Contrast active equipment.
passive transfer <i>n</i>	<i>in automated material movement</i> , a transfer that involves one active and one passive partner. During a passive transfer, the active partner retains control of the transfer envelope during the entire physical transfer. [SEMI E32-94]
passive transfer partner <i>n</i>	<i>in automated material movement</i> , a transfer partner that takes no part in the physical micro level transfer, moving nothing within the transfer envelope. NOTE- This term refers to the physical micro level transfer phase only. Setup activities prior to the transfer may be performed by a passive transfer partner; for example, a port door may be opened during setup phase. [Adapted from SEMI E32-94] Contrast with active transfer partner.
pattern deformation <i>n</i>	<i>in dielectrically isolated (DI) wafers</i> , a microscopic defect associated with missing or indented tub features of 4 microns or more. [SEMI M22-92]
pattern dimension precision and accuracy <i>n</i>	critical dimension (CD) variation and deviation of written pattern from designed value. [SEMI P21-92]

WOLF Reference

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 2:
PROCESS INTEGRATION**

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MULTILEVEL-INTERCONNECT TECHNOLOGY FOR VLSI AND ULSI 273

- PECVD TEOS film, deposited at 330°C. (Figure 4-54c shows that the resulting hillock size and density are both small.)¹⁷²
- ECR deposition (see section 4.4.10).
- Photo-CVD SiO₂.¹⁸³
- Afterglow-CVD of SiO₂.²⁴
- Anodized Al deposition.¹⁸⁴

Once such dielectric films are in place, they suppress hillock growth during later thermal cycling.

- *Use of refractory metal films such as W or Mo (which exhibit much less propensity to form hillocks at 400°-500°C) in place of Al.*
- *Use of an ionized cluster beam deposition process to deposit smooth Al/CaF₂/Si films.* According to the report on this process, the films remained hillock free up to temperatures of 500°C.¹⁸⁵

4.7.4.2 Dielectric Void Reliability Problems. If the voids are opened following an etchback step, they can trap moisture or photoresist residues that can cause long term reliability problems. In addition, metal may be deposited into the voids that can be very difficult to remove by etching, thus producing shorting between neighboring metal lines.

4.8 PASSIVATION LAYERS

Following patterning of the final metal layer, a *passivation layer* is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging. The desired properties of the passivation materials are given in Table 4-5. In general, the thicker the passivation layer the better, since a thicker layer will provide better protection and improve the electromigration resistance of underlying Al lines. On the other hand, because thicker CVD films (especially silicon nitride films) have a higher tendency to crack, there is normally an upper limit to the thickness.

The final mask, called the *pad mask* or *bonding contact mask*, is used to define patterns corresponding to the regions in which electrical contact to the finished circuit will be made. These patterns in a resist layer allow openings in the passivation layer to be etched down to Al areas on the circuit called bonding pads (see chap. 5, Fig. 5-16). Either wet or dry etching can be used to etch the passivation layer. Since the dimensions of the pads are so large (i.e., normally 100 x 100 μm), wet etching is still frequently used to etch PSG films, while silicon nitride films are more easily etched by means of a dry etching process.

Phosphorus-doped, low-temperature CVD SiO₂ films were the first passivation layers to be used. The phosphorus is added to the SiO₂ to reduce the stresses in the film (and to thereby decrease the tendency of the film to crack), as well as to improve the gettering

274 SILICON PROCESSING FOR THE VLSI ERA - VOLUME II

properties of the film (with respect to sodium ions and other fast-diffusing metallic contaminants). The higher the phosphorus concentration, the better these characteristics will be.

On the other hand, if more than 6 wt% phosphorus is added to the film, corrosion can become a serious problem, especially in the case of chips mounted in plastic, nonhermetic packages. Water vapor can rapidly penetrate the plastic packaging material, transporting with it contaminants from the surface of the package. If the PSG contains excess phosphorus, the moisture can react with it to form phosphoric acid (HPO_3), which will eventually penetrate the film. As noted earlier, electrochemical corrosion of the Al lines can lead to metallization failure. While the transport of contaminated moisture through the PSG is a relatively slow process, if cracks or defects (e.g., pinholes) exist in the film, the water vapor will be able to penetrate it much more rapidly.

Silicon nitride has also been used as a passivation-layer material because it provides an impermeable barrier to moisture and mobile impurities (e.g., sodium) and also forms a tough coat that protects the chips against scratching. Its high dielectric constant is not a disadvantage for this application, since the passivation layer is deposited on top of the last metal layer.

However, because the passivation layer must be deposited over Al films, only PECVD silicon nitride can be used for this application (since it is deposited at $\sim 300^\circ\text{C}$). Unfortunately, PECVD nitride films normally exhibit a high mechanical stress ($\sim 6\text{--}8 \times 10^8 \text{ Pa}$), which can cause cracks in the film during heating after deposition (especially at steps). The high compressive stresses in the films have also been shown to enhance void formation in Al interconnects (see section 4.7).

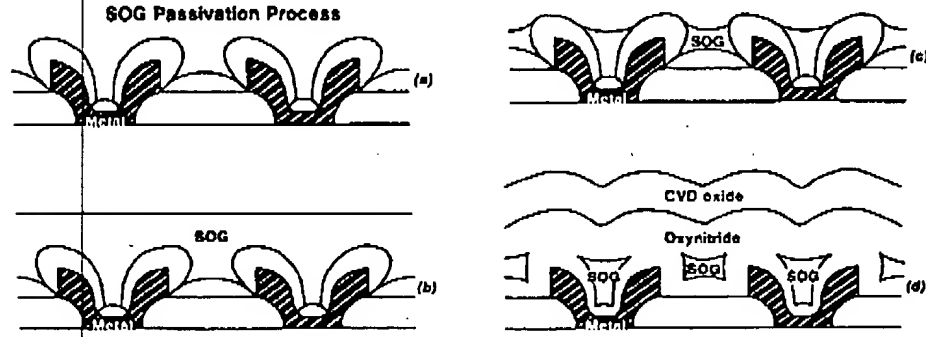
In addition, PECVD silicon nitride tends to be nonstoichiometric and contains substantial quantities of atomic hydrogen (10–30 at%). Large quantities of hydrogen have been found to accelerate hot-electron aging effects in MOS devices (see section 5.6.6). It has also been reported that the hydrogen from PECVD nitride is responsible for the formation of bubbles or cavities at the metal–plasma nitride interface when Al:Si alloys are used as the metallization. These appear after the 450°C anneal that is carried out following nitride deposition. It is supposed that the hydrogen reacts with the Si precipitates in the Al film to form gaseous compounds that produce the bubbles.^{186,187} It has been recommended that a low-hydrogen-content passivation film be used, if nitride passivation is selected for MOS technologies with gate lengths of less than $1.5 \mu\text{m}$ (in which hot-electron degradation is significant).

Work has been done to develop processes for growing nitride films with low hydrogen concentration and stress, and more is now understood about the relationship of the film properties to such deposition conditions as rf frequency, power, and bias.¹⁸⁸ Lower H_2 concentrations in the nitride have been obtained when the film is formed with $\text{SiH}_4\text{--N}_2$ mixtures rather than with conventional $\text{SiH}_4\text{--NH}_3$ mixtures.¹⁸⁹ Fluorinated nitride (F-SiN) films have been developed that exhibit only 0.6% of hydrogen (in the form of Si-H).^{190,191}

The use of PECVD silicon-oxynitride films (deposited with SiH_4 , NH_3 , N_2 , and N_2O mixtures) as alternative passivation materials has also been investigated, since they exhibit nearly the same the moisture and sodium barrier characteristics of nitrides.

MULTILEVEL-INTERCONNECT TECHNOLOGY FOR VLSI AND ULSI 275

SOG Passivation Process



1. (a) Deposition of the first oxynitride layer. (b) SOG passivation process after second oxynitride and applied. (c) after SOG etch back, and (d) finished CVD oxide depositions.

Fig. 4-56 Using SOG film as a part of the passivation overcoat improves EPROM reliability.²⁵⁶ Reprinted with permission of Semiconductor International.

While not quite as good as those of nitrides, the characteristics are better than those of oxides.¹⁹² However, their stress is between that of APCVD oxide (tensile) and plasma nitride and oxide (compressive).¹⁹³ In addition, because the stress is a function of applied rf power, pressure, and bias, it is possible to optimize the stress by using bias. Ideally, a very low-stress dielectric oxynitride film can be formed that will still maintain good diffusion-barrier properties. (It is important to characterize the stress over the entire temperature range of operation to which the dielectric film will be subjected, since the stress can exhibit hysteresis effects. These may be due to structural changes in the film due to loss of material during heating.) Finally, it is reported that PECVD oxynitride films can be formed that contain considerably less H_2 (~one-half, in one report) than do PECVD nitrides.¹⁹⁴

Another, more recently adopted approach to the formation of passivation layers involves multilayer passivation coating. An initial coating of PECVD oxide is deposited, followed by a PECVD nitride. The oxide layer reduces the mechanical stress (~40%) and the hydrogen content of the passivation layer, while the nitride protects the device against handling, humidity, and mobile ions. This inorganic bilayer may be followed by a polyimide layer that is several microns thick (especially useful in automated bump-bonding processes) and a thick layer of silicone gel, or similar material, for cushioning and for void elimination during die bonding.

In a second variation of this technique applied to EPROMs, a sandwich oxynitride-(etchedback) SOG-oxynitride layer is first formed. This film is then covered with a low phosphorus-content CVD-oxide layer to complete the composite passivation film (Fig. 4-56). Sandwiching the SOG film between the two oxynitride layers reduces the occurrence of voids and seams in the passivation layer. These voids and seams caused degraded passivation film coverage, which in turn correlated with increased EPROM array failures after steam stressing.²⁵⁶

276 SILICON PROCESSING FOR THE VLSI ERA - VOLUME II

Table 4.5 Desired Properties of a Passivation-Layer Material

1. Provides good scratch protection to underlying circuit structures. In general, the thicker the passivation layer the better, subject to cracking and patterning restrictions.
2. Impermeable to moisture, as moisture is one of the main catalysts for corrosion.
3. Exhibits low stress, preferably compressive ($\sim 5 \times 10^8$ dynes/cm²).
4. Conformal step coverage.
5. High thickness uniformity.
6. Impermeable to sodium atoms and other highly mobile impurities.
7. Easily patterned.
8. Good adhesion to conductors, as well as to the interlevel dielectric beneath the last level of metal.

4.9 SURVEY OF MULTILEVEL METAL SYSTEMS

As noted earlier, with NMOS IC technology it was possible to exploit the polysilicon layer as an extra level of interconnect, while in bipolar technology it was necessary to develop a two-level-metal system in order to obtain comparable flexibility of interconnect routing. As a result, the problems of two-level-metal systems (primarily, the implementation of low-temperature planarization techniques) first had to be tackled by bipolar IC manufacturers. When CMOS replaced NMOS as the dominant MOS VLSI technology, CMOS ICs also required a two-level-metal system, since the polysilicon could not perform the function of a local interconnect level as effectively as it had in NMOS (see chaps. 2 and 6). However, the polysilicon gate structures and the nonrecessed LOCOS field-oxide steps in CMOS created an even more difficult topography for two-level-metal CMOS systems than for bipolar systems.

4.9.1 Bipolar Double-Level-Metal Systems

The first example we present is that of a structure described in 1984 by Ghate et al. of Texas Instruments.¹⁹⁵ The Metal-1 pitch is 4 μm , and the Metal-2 pitch is 6 μm . Metal 1 is a 575-nm-thick bilayer film of Ti:W covered with Al:Cu, and the contact to silicon is made by self-aligned PtSi formed in the contact holes. Metal 2 is also a bilayer film of Ti:W and Al:Cu, 775 nm thick. The intermetal-dielectric layer is a 600-nm-thick PECVD oxide layer in which 1.1- μm vias are opened to allow contact between Metal 2 and Metal 1. No planarization of the intermetal dielectric was reported for this DLM process.

A second example, detailed by Bergeron et al. of IBM, uses a bilayer PECVD silicon-nitride/polyimide film as the intermetal dielectric. Smoothing of the underlying metal topography is achieved through use of the polyimide.¹⁹⁶ The Metal-1 pitch is 5 μm and the Metal-2 pitch is 7.0 μm . Metal 1 and Metal 2 are both Al:4%Cu films defined by lift-off, and Metal 2 is 2 μm thick. The bilayer intermetal-dielectric film is etched by

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